AC37 HIGH-SPEED COMMUNICATION ADAPTER CARD USER'S GUIDE

Form 461-021028 — October, 2002

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Opto 22 warrants all of its products to be free from defects in material or workmanship for 30 months from the manufacturing date code. This warranty is limited to the original cost of the unit only and does not cover installation, labor, or any other contingent costs. Opto 22 I/O modules and solid-state relays with date codes of 1/96 or later are guaranteed for life. This lifetime warranty excludes reed relay, SNAP serial communication modules, SNAP PID modules, and modules that contain mechanical contacts or switches. Opto 22 does not warrant any product, components, or parts not manufactured by Opto 22; for these items, the warranty from the original manufacturer applies. These products include, but are not limited to, the OptoTerminal-G70, OptoTerminal-G75, and Sony Ericsson GT-48; see the product data sheet for specific warranty information. Refer to Opto 22 form number 1042 for complete warranty information.

TABLE OF CONTENTS

WELCOME

ABOUT THIS MANUAL

This manual is organized as follows:

- **Chapter 1: AC37: IBM AT to Remote Bus Adapter Card**
- **Chapter 2: Register Definition**
- **Chapter 3: External Interrupt Line, Remote I/O IRQ**
- **Chapter 4: Mode of Operation**

DOCUMENT CONVENTIONS

- **Bold** typeface indicates text to be typed. Unless otherwise noted, such text may be entered in upper or lower case. (Example: "At the DOS prompt, type **cd\windows**.")
- *Italic* typeface indicates emphasis and is used for book titles. (Example: "See the *OptoControl User's Guide* for details.")
- File names appear in all capital letters. (Example: "Open the file TEST1.TXT.")
- Key names appear in small capital letters. (Example: "Press SHIFT.")
- Key press combinations are indicated by plus signs between two or more key names. For example, SHIFT+F1 is the result of holding down the SHIFT key, then pressing and releasing the F1 key. Similarly, CTRL+ALT+DELETE is the result of pressing and holding the CTRL and ALT keys, then pressing and releasing the DELETE key.
- "Press" (or "click") means press and release when used in reference to a mouse button.
- Menu commands are sometimes referred to with the Menu→Command convention. For example, "Select File→Run" means to select the Run command from the File menu.
- Numbered lists indicate procedures to be followed sequentially. Bulleted lists (such as this one) provide general information.

AC37: IBM AT TO REMOTE BUS ADAPTER CARD

The AC37 is a computer adapter card that provides a RS-485 2 or 4-wire communications link. It is designed to allow any IBM AT or compatible computer access to the Opto 22 Remote I/O Bus. The Remote Bus is a standard RS-485 half-duplex (2 wire) serial communications link. The AC37 is primarily used to allow an AT to be the host on a Remote Bus link controlling a network of Opto 22 Remote I/O bricks, though it can also be used to monitor a link for redundant host applications.

The AC37 is designed to appear as a standard IBM serial 'COM' port to user software. The CPU accessible registers are arranged and addressed in the same order as the registers of the 16,450 / 16,550 UART chip normally used on AT serial ports. While not all of the functions of the 16,550 are supported (e.g., modem control), all registers necessary for Remote Bus communications are configured in the same manner as a serial port.

SUMMARY OF FEATURES:

- Serial link baud rates to 460,800
- Remote bus interrupt input capability
- RS-485 2-wire, half-duplex or 4-wire, full-duplex operation
- Serial and IRQ lines transient protected
- Serial and IRQ lines optically isolated to 2,500 VAC
- Up to 3,000 feet of cable length using twisted pair cable at 115,200 baud
- Multidrop capability, RS-485 balanced line drivers
- Transmit, Receive, IRQ, and run LED indicators
- The AC37 has a CPU on it which allows it to handle high speed serial communications tasks for the host CPU. The firmware program run by the AC37 CPU allows it to operate and appear to the host CPU as a standard serial 'COM' port AC37 CPU features include:

    80C196KR 16 Bit High Performance Microcontroller

    64 KB EPROM

    Two 512 byte FIFOs for Data Transfers to/from Host CPU

ADDRESS SELECTION:

There are seven address jumpers on the AC37 labeled A3 through A9. These jumpers are used to select the base address of the adapter card.The IBM PC-AT and compatibles only use 10 address lines for addressing I/O locations. Since the AC37 card uses the three lower address lines directly, the upper seven (A3 through A9) are used to decode the base address of the card.

Address jumpers A3 through A9 correspond to address lines A3 through A9. When a jumper is installed, the jumper value is zero. A jumper not installed will indicate a one. When the address lines of the AT match the jumper settings, the card is selected.

The base address must be less than 3FF Hex and have a zero or eight as the last digit. Care should be taken to select a base address which will not conflict with other devices in the system.

Sample addresses and jumper settings are shown below:

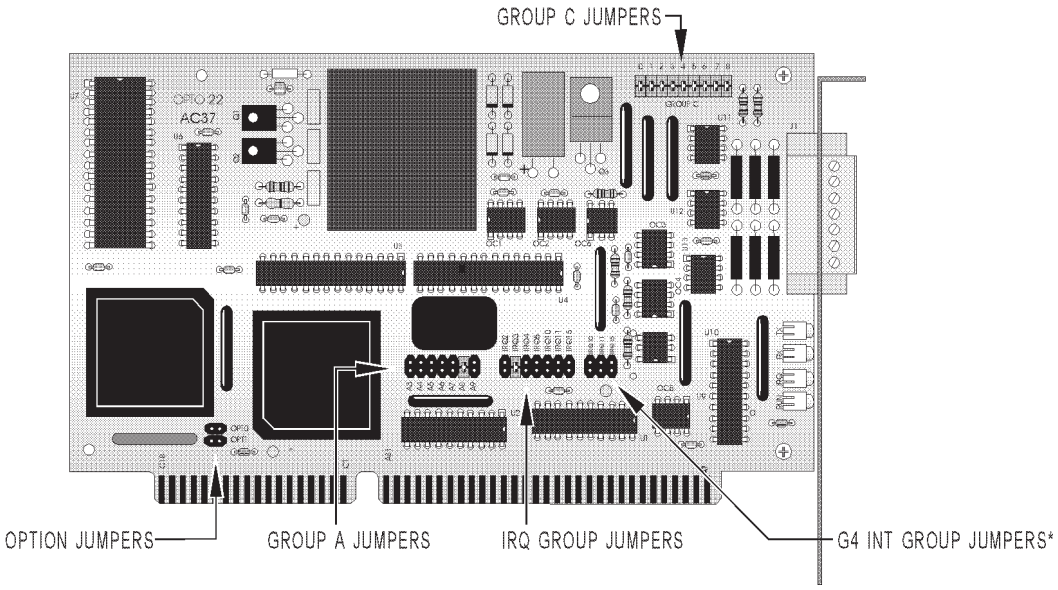
Port	Hex Address	A Group Jumpers							IRQ Group Jumper	G4 Int Select Jumper
		A9	A8	A7	A6	A5	A4	A3		
COM1	3F8	0	0	0	0	0	0	0	IRQ4	IRQ15
COM2	2F8	0	X	0	0	0	0	0	IRQ3	IRQ15
COM3	3E8	0	0	0	0	0	X	0	IRQ4	IRQ15
COM4	2E8	0	X	0	0	0	X	0	IRQ3	IRQ15
OPTO COM3	348	0	0	X	0	X	X	0	IRQ2	IRQ15
OPTO COM4	340	0	0	X	0	X	X	X	IRQ5	IRQ15
OPTO COM5	248	0	X	X	0	X	X	0	IRQ10	IRQ15
OPTO COM6	240	0	X	X	0	X	X	X	IRQ11	IRQ15

X = Jumper installed

0 = Jumper not installed

HOST CPU INTERRUPT REQUEST LINE SELECTION:

The AC37 allows for the selection of the interrupt request line with a group of jumpers labeled 'IRQ GROUP'. All of the interrupts found in the Interrupt Identification Register can be routed to one interrupt request line by installing the jumper for that line. Only one jumper should be installed in this group, and care should be taken to insure that no other device is using the selected interrupt request line.



* Do not install any jumpers here if using Cyrano software.
See page 1-6 if you need these features.

RS-485 SERIAL LINE TERMINATION AND BIASING:

The nine jumpers on the AC37 labeled 'GROUP C' are used to install transmission line terminators and/or tri-state biasing resistors as needed. The function of each jumper is as follows:

Jumper C0: Pull-up for TX/RX + line

Jumper C1: Terminator for TX/RX lines

Jumper C2: Pull-down for TX/RX - line

Jumper C3: Pull-up for RX+ line

Jumper C4: Terminator for RX lines

Jumper C5: Pull-down for RX- line

Jumper C6: Pull-up for IRQ + line

Jumper C7: Terminator for IRQ lines

Jumper C8: Pull-down for IRQ - line

Terminating resistors should always be installed at both ENDS of an RS-485 transmission line, and the line must have only TWO ends. The biasing resistors are only necessary at one place on the line and are typically installed at the host.

EXAMPLES:

If the AC37 is communicating to a Mistic Model 200 Processor (G4LC32) and is located at one end of the line, install C1, C3, C5, C6, and C8.

If the AC37 is the host (master) of a Remote I/O Bus and is located at one end of the line, ALL group C jumpers should be installed.

If the AC37 is to be the host of a Remote I/O Bus and is NOT located at one end of the line, install jumpers C0, C2, C3, C5, C6, and C8 only. Terminating resistors must be installed at both ends of the transmission lines.

If the AC37 is to be a redundant or passive host which is monitoring a 2-wire Remote I/O link, and is not at one end of the link, install jumpers on C3 and C5 and remove all other C group jumpers.

INSTALLATION:

After jumpering, the AC37 is ready for installation in any AT class (286, 386, or 486) machine. The AC37 requires a 16-bit slot in the computer.

To install:

1) Remove computer cover

2) Insert AC37 in any 16-bit slot

3) Screw AC37 retainer bracket to case

4) Replace computer cover

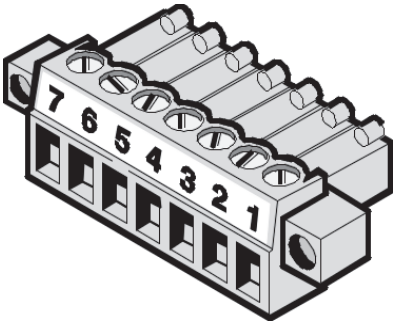
CABLE:

RS-485 serial lines require twisted pair cable. Maximum cable length is 3,000 feet. The recommended cable type is 2 twisted pair of 24 gauge conductors with a shield. Nominal impedance is 100 ohms and capacitance is 12.5 picofarads per foot. Typical manufacturer part numbers are:

Manhattan Electric Cable	M3475
Belden Wire and Cable	9,729

CONNECTOR PIN ASSIGNMENTS

The removable cable plug connector is Phoenix Contact p/n MC 1,5/7-STF-3,81.



Pin	Description
1	TX/RX+ (2-wire) or TX+ (4-wire)
2	TX/RX- (2-wire) or TX- (4-wire)
3	COMMON
4	RX+ (4-wire)
5	RX- (4-wire)
6	IRQ+
7	IRQ-

OPTION JUMPERS

Option jumper 0 selects the AC37's operation mode. Typically, mode 0 is used when data is received in the communications buffer on a character by character basis. Mode 0 enables the AC37 to function like any standard serial COM port (16,550 UART, emulation mode 0). Mode 1 is used when a complete data response is received and ready in the communication buffer.

Remove jumper 0 to set the AC37 to mode 0 for connections to Mistic I/O bricks. If you are using the AC37 with Mistic MMI or Cyrano to a Mistic controller, install jumper 0. This sets the AC37 to mode 1. For more about the option jumpers, see the "Modes of Operation" section.

Option jumper 1 is reserved for future use.

REGISTER DEFINITION

The CPU accessible registers are addressed as follows:

Offset from Base Address	DLAB * State	Register Function	Type
0	0	Receive Buffer	Read Only
0	0	Transmit Buffer	Write Only
0	1	Baud Rate Select	Read/Write
1	0	Interrupt Enable	Read/Write
2	X	Interrupt Identification	Read Only
2	X	Reset Control	Write Only
3	X	Line Control	Read/Write
5	X	Line Status	Read Only
6	X	Modem Status	Read Only
7	X	Card Identification	Read Only
	X = Don't Care		

* The DLAB (Divisor Latch Access Bit) is bit 7 of the Line Control Register.

TRANSMIT BUFFER REGISTER: OFFSET 0 - WRITE ONLY

Data written to the transmit register is put into a 512 byte deep FIFO (First In First Out) memory. The CPU on the AC37 then reads and transmits the data out the RS-485 port.

RECEIVE BUFFER REGISTER: OFFSET 0 - READ ONLY

This register is used to read data received on the RS-485 port. Remote Bus data received is buffered in a 512 byte deep FIFO (First In First Out) memory.

CARD IDENTIFICATION REGISTER: OFFSET 7 - READ ONLY

This register will always read as 37 Hex, which may be used by software to identify the port as an AC37. Writing to this address will have no effect.

BAUD RATE SELECT REGISTER — OFFSET 0 - READ/WRITE

This register is used to select the baud rate for the RS-485 serial communications. This register corresponds to the least significant byte of the divisor latch in a 16,550 UART and may be configured in the same manner with the same results. The DLAB bit in the Line Control Register must be set to a 1 before this register can be accessed. If the Baud Rate Select Register is configured to something other than the selections shown below, a default baud rate of 115,200 will be set.

Desired Baud Rate	Baud Rate Select Register Setting
110	17 Hex
150	00 Hex
300	80 Hex
600	C0 Hex
1,200	60 Hex
2,400	30 Hex
4,800	18 Hex
9,600	0C Hex
19,200	06 Hex
38,400	03 Hex
57600	02 Hex
76,800	F0 Hex
115,200	01 Hex
153,600	F4 Hex*
230,400	F3 Hex*
307,200	F5 Hex *
460,800	F6 Hex *

* Not Used with Mistic Remote I/O systems.

INTERRUPT ENABLE REGISTER: OFFSET 1 - READ/WRITE

This register is used to enable or disable the various types of host CPU interrupts which can be generated by the AC37. Disabling an interrupt prevents it from being indicated as active in the Interrupt Identification Register and from activating the host CPU interrupt line. All other system functions operate in their normal manner, regardless of their interrupt enable status. The Interrupt Enable Register is defined below:

Bit 0: Received Data Available Interrupt Enable
When set to a logic 1, a received data available interrupt is generated whenever the Receive Data Available bit is set in the Line Status Register. Refer to the description of the Receive Data Available bit in the Line Status Register.

Bit 1: Transmit Buffer Register Empty Interrupt Enable
When set to logic 1, a transmit buffer empty interrupt is generated whenever the transmit FIFO is ready to accept data. Refer to the description of the Transmit Buffer Empty flag (bit 5) in the Line Status Register.

Bit 2: Receiver Line Status Interrupt Enable
When set to a logic 1, a receiver line status interrupt is generated upon a receive buffer overrun error or a framing error. A receive buffer overrun error occurs when a data byte is received while the receive FIFO is full. A framing error occurs if a stop bit was not received at the appropriate time.

Bit 3: Modem Status Interrupt Enable
When set to a logic 1, a modem status interrupt is generated when the IRQ line of the Remote Bus is activated. Since the AC37 has no modem support, the Remote Bus IRQ line is directed through what is normally the CTS status bit.

Bits 4–7: Not Used
These bits are not used. They cannot be written to and will always read as zero.

INTERRUPT IDENTIFICATION REGISTER: OFFSET 2 – READ ONLY

This register can be read to determine if any interrupts are currently pending, and if so, what type. The AC37 prioritizes interrupts into the same four levels that the 16,550 UART does. The interrupt order of priority is:

1) Receiver Line Status

2) Receive Data Available

3) Transmit Buffer Empty, and 4) Modem Status. The Interrupt ID Register bits are defined below:

Bit 0: When this bit reads as a logic 0, an interrupt is pending and the contents of the Interrupt ID Register can be used to vector to the appropriate interrupt service routine.

Bits 1–2: These two bits are used to identify the highest priority interrupt pending. The four types are identified per the table below.

Bits 3–7: These bits are not used and will always read as logic 0.

Bit 2	Bit 1	Bit 0	Priority	Interrupt Type
0	0	1		No Interrupt Pending
1	1	0	Highest	Line Status Interrupt
1	0	0	Second	Receive Data Available
0	1	0	Third	Transmit Buffer Empty
0	0	0	Fourth	Modem Status

A Line Status Interrupt is generated by either a receive buffer overrun or framing error. Refer to the Line Status Register definition for a description of these errors. A Line Status Interrupt is cleared by reading the Line Status Register.

A Receive Data Available Interrupt is generated whenever the Receive Data Available bit is set in the Line Status Register. This interrupt is cleared by reading all data from the receive buffer or by resetting the FIFO. Refer to the description of the Receive Data Available flag (bit 0) in the Line Status Register.

A Transmit Buffer Empty Interrupt is generated whenever the transmit FIFO is ready to receive data. Refer to the description of the Transmit Buffer Empty flag (bit 5) in the Line Status Register.

A Modem Status Interrupt is generated by the Remote Bus IRQ line being active. Since the AC37 is not intended for use with modems, the Remote Bus IRQ line is directed through what is normally the CTS bit on the 16,550 UART. This interrupt is cleared by deactivating the Remote Bus IRQ line.

RESET CONTROL REGISTER: OFFSET 2 - WRITE ONLY

This register is used to control the reset functions of the AC37. The bits of the Reset Control Register have the following functions:

Bit 0: Not Used

Bit 1: Receive FIFO Reset
Writing a logic 1 to this bit will reset the receive FIFO. All data in the FIFO will be cleared and it's pointers reset to 0. Data being shifted into the receiver is not affected. This bit is self clearing and it is not necessary to write a logic 0 afterward.

Bit 2: Transmit FIFO Reset
Writing a logic 1 to this bit will reset the transmit FIFO. All data in the FIFO will be cleared and it's pointers reset to 0. Data being shifted out of the transmitter is not affected. This bit is self clearing and it is not necessary to write a logic 0 afterward.

Bit 3: Not Used

Bit 4: CPU Reset
To reset the AC37 CPU, write a logic 1 to Bit 4 and verify the DLAB bit in the Line Control is set to 1. This will have the same affect as cycling power to the AC37. Both receive and transmit FIFOs are also reset. Baud Rate, Interrupt Control and Line Control registers will be cleared and need reconfiguring by the host CPU. Since the reset cycle can take two seconds, the host CPU should not try to reconfigure the AC37 registers until 2 seconds after initiating a reset. This bit is self clearing and it is not necessary to write a logic 0 afterward.

Bit 5: Not Used

Bit 6: Not Used

Bit 7: Not Used

LINE CONTROL REGISTER: OFFSET 3 - READ/WRITE

This register is used to select the format of serial communications data. The bits in the Line Control Register are defined as such:

Bits 0 and 3: Word Size Select

These two bits specify the number of bits in each serial character sent or received. The AC37 does not support all of the various word sizes that the 16,550 UART does, but the most commonly used data formats are supported and are selected using the settings shown below:

Bit 3	Bit 0	Format
1	1	9 Data Bits, 1 Stop Bit *
0	1	8 Data Bits, 1 Stop Bit **
1	0	7 Data Bits, 1 Parity Bit, 1 Stop B
		(Parity will always be even)
0	0	Reserved

* 9 Bit mode is used to communicate to Remote I/O using binary protocol.

** 8 Bit mode is used to communicate to Remote I/O using ASCII protocol.

Bit 1: Not Used

Bit 2: Not Used

Bit 4: Address-/Data Select

This bit controls the state of the 9th data bit when the 9 bit mode is selected. When communicating to a Remote I/O brick using binary protocol, this bit determines if the next byte written to the transmit FIFO will be interpreted as an address or data byte. If bit 4 is set to a logic 0, the 9th bit of data written to the transmit FIFO will be set to a logic 1 when transmitted, and will be interpreted as an address byte by the Remote I/O. Conversely, if bit 4 is set to a logic 1, the 9th bit of data written to the transmit FIFO will be set to a logic 0 when transmitted and interpreted by the Remote I/O as data bytes.

Bit 5: Not Used

Bit 6: IRQ Output Control

This bit controls the state of the Remote Bus IRQ line. When bit 6 is set to a logic 1, the IRQ line of the Remote Bus is activated. When bit 6 is set to a logic 0, the IRQ line will be put into receive mode.

Bit 7: DLAB Control

This bit is used to control access to the Baud Rate Select Register. If this bit is set to a logic 0, the Receive buffer, Transmit buffer, and Interrupt Enable register may be accessed. If this bit is set to a logic 1, only the Baud Rate Select register may be accessed at offset 0.

MODEM CONTROL REGISTER: OFFSET 4 – READ/WRITE

This register is associated with modems in name only. The AC37 does not support modem control. This register has been provided to support other features, in this case the secondary interrupt. The secondary interrupt feature on AC37 is used by the Remote Bus IRQ line. Only one bit in the register is used for this purpose; other bits are not used.

There are two basic versions of the AC37 in the field: an older full-length card and a newer half-size card. The newer card supports the use of this bit to enable interrupts. The older AC37 does not support the use of this bit; however, we recommend that the bit still be set to ensure compatibility with all versions.

NOTE: If you are using Windows NT, you must use the newer AC37, and its U5 must be labeled 9087. Earlier versions will not work with NT.

Bits 0–2:	Not Used
Bit 3:	Secondary Interrupt Enable This bit is cleared upon power-up reset and must be set for the secondary interrupt to be enabled.
Bits 4–7:	Not Used

LINE STATUS REGISTER: OFFSET 5 - READ ONLY

This register can be read to obtain the current status of the receive or transmit buffers. The function of each bit is described below:

Bit 0: Receive Data Available
When the AC37 is operating in mode 0*, this bit will be set to a logic 1 whenever the receive FIFO has data in it. When the AC37 is operating in mode 1*, this bit will be held to a logic 0 until the last character of a Remote I/O command response is put into the receive buffer. Bit 0 can be reset to a logic 0 by either reading all the data from the receive buffer or by resetting the FIFO. The receive FIFO is 512 bytes deep.

* Refer to the section on Modes of Operation for a more detailed explanation of the different operating modes.

Bit 1: Overrun Error Indicator
This bit is set to a logic 1 whenever the CPU of the AC37 attempts to put data into the receive FIFO while it is full. When this occurs, the data currently in the FIFO is unaffected but the incoming data is lost. The receive FIFO is 512 bytes deep. The Overrun Error Indicator is reset to a logic 0 when the Line Status Register is read.

Bit 2: Not Used
This bit is not used and will always read as a logic 0.

Bit 3: Framing Error, Overrun Error, Parity Error Indicator
This bit is set only when the the CPU of the AC37 experiences a framing error, overrun error, or parity error while receiving data. This bit is cleared when the Line Status Register is read.

Bit 4: Not Used
This bit is not used and will always read as a logic 0.

Bit 5: Transmit Buffer Empty
Bit 5 is set whenever the transmit FIFO is ready to accept data. The transmit FIFO is 512 bytes deep. When the transmit FIFO becomes full, this bit is set to a logic zero. It will remain set to a logic zero until enough data has been transmitted to cause the FIFO to only be half full.

Bit 6: Transmit Driver Active
This bit is set to a logic 0 while the AC37 is transmitting data. This bit is set to a logic 1 when the AC37 is not transmitting and is ready to receive data.

Bit 7: Not Used
This bit is not used and will always read as a logic 0.

MODEM STATUS REGISTER: OFFSET 6 - READ ONLY

This register is associated with modems in name only. The AC37 does not support modem control, but this register has been provided to allow the status of other features to be obtained. The bits are defined below:

Bit 0: IRQ Line Status
This bit is set to a logic 1 whenever the Remote Bus IRQ line is being driven to the active state by a device other than the AC37. Bit 0 functions identically to bit 4.

Bit 1: Not Used
This bit is not used and will always read as a logic 0.

Bit 2: CPU Interrupt Request
This bit is set to a logic 1 when the CPU of the AC37 is requesting to interrupt the host CPU. This feature is for future product enhancements. Current operating modes of the AC37 will not generate this interrupt and this bit will read as a logic 0. Bit 2 functions identically to bit 6.

Bit 3: Not Used
This bit is not used and will always read as a logic 0.

Bit 4: IRQ Line Status
This bit is set to a logic 1 whenever the Remote Bus IRQ line is being driven to the active state by a device other than the AC37. Bit 4 functions identically to bit 0. Bit 4 is the CTS status bit in a 16,550 UART chip.

Bit 5: Address/Data Receive Flag
When the AC37 is operating in 9 bit mode, this bit is used to indicate the status of the 9th bit of the last byte read from the receive FIFO. If the AC37 is being used to monitor a Remote I/O link using binary protocol, this bit will indicate whether the received byte was an address or data. If the last byte read was an address byte, bit 5 will be set to a logic 1. Bit 5 will be set to a logic 0 if the last byte read from the receive FIFO was designated as a data byte. The status of this bit is only affected by a read from the receive FIFO.

Bit 6: CPU Interrupt Request
This bit is set to a logic 1 when the CPU of the AC37 is requesting to interrupt the host CPU. This feature is for future product enhancements. Current operating modes of the AC37 will not generate this interrupt and this bit will read as a logic 0. Bit 6 functions identically to bit 2.

Bit 7: Not Used
This bit is not used and will always read as a logic 0.

EXTERNAL INTERRUPT LINE, REMOTE I/O IRQ

The IRQ lines on the Phoenix connector are a bi-directional RS-485 link which are normally set as inputs. They are meant to be used with the IRQ output lines found on Remote I/O bricks. The IRQ outputs of Remote I/O bricks are RS-485 drivers which are held in tri-state mode until an interrupt is requested, at which time the outputs are enabled and set active. The AC37 will receive this signal and set the IRQ Line Status bit in the Modem Status Register. If enabled, this will cause a modem status interrupt to be generated.

The G4INT jumper group is provided to allow the external interrupt to be routed to a unique host CPU interrupt request line. This may be necessary if communications software cannot implement the use of a 'Clear To Send' interrupt as the external (Remote I/O) interrupt handler. By installing a jumper in the G4INT group, and disabling the modem status interrupt in the Interrupt Enable Register, the user may utilize separate interrupt request lines (with unique vectors and routines) for the serial communications and external interrupt handling. The G4INT jumper will directly route the external interrupt signal to the selected interrupt request line, and it may only be enabled or disabled by the interrupt controller of the host AT. If used, only one jumper should be installed in the G4INT group, and the user should be certain that the interrupt request line selected is not used by any other device, including the IRQ GROUP selection.

Before a Remote I/O brick can generate an interrupt, a number of commands must be executed. These are:

1. Set Event Table Entry
   An entry must be made instructing the I/O brick to monitor for a specific event occurrence.

2. Enable Event Table Entry
   The event entry must be enabled for scanning by the I/O brick.

3. Set Event Interrupt Status
   The event entry interrupt must be enabled.

4. Set System Options
   The Global Interrupt Enable bit must be set.

And, of course, the event being monitored must then occur.

An interrupt from a Remote I/O brick is cleared by executing a 'Read and Clear Event Latches' command. All event entries on a specific brick which are set to generate an interrupt should be specified when reading and clearing as the interrupt output is cleared by the command.

MODES OF OPERATION

The AC37 has two operating modes. Mode 0 is selected by removing the OPT0 (OPTION 0) jumper. Mode 1 is selected by installing the OPT0 jumper. Option jumper 1 is reserved for future use. The option jumpers are read only after the AC37 has been powered up or upon reset.

Mode 0:

While in mode 0, the AC37 will operate very much like a standard serial COM port. It also will not receive what it has transmitted. When data is received, it is put into the receive FIFO and the Receive Data Available bit is set immediately. This bit remains set until all data has been read from the receive FIFO or the FIFO is reset. When data is put into the transmit FIFO, it is read and transmitted as room becomes available in the output shift register.

Mode 1:

Mode 1 is intended to facilitate the command-response transactions necessary to operate Remote I/O bricks. This is done primarily by holding the Receive Data Available flag reset until the complete response string is put into the receive FIFO. By doing so, the AC37 minimizes the time required for the host CPU to collect the data, since only one interrupt is necessary to read the entire response. Both ASCII and binary protocols are supported and the operation of the AC37 will be slightly different depending on which is being used.

ASCII Protocol:

The AC37 will send and receive data much the same way as it does in mode 0, except that after transmitting a carriage return (the ASCII protocol end-of-message character), the AC37 will stop transmitting and wait for a response from the Remote I/O brick or controller. As the response string is received, it is put into the receive FIFO but the Receive Data Available bit is held clear until a carriage return is received. If a receive error occurs, or two seconds expire with no data having been received, the Receive Data Available flag is allowed to operate in it's normal manner.

Binary Protocol:

The binary protocol uses 9 bit characters to transfer data to and from the Remote I/O bricks and controllers. The 9th bit is used to differentiate data bytes from address bytes. Address bytes are normally only sent at the beginning of a command string.

In mode 1, when the AC37 reads an address byte from the transmit FIFO it will wait to transmit the address byte until the second byte (count byte) is put into the transmit FIFO. This has the effect of holding off the Transmit Driver Active flag (normally the Transmit Shift Register Empty flag), and allowing the software to change the state of the 9th bit without waiting for the first byte to be completely shifted out. While this is not necessary when using the AC37, it may be done to keep software compatible with other serial cards.

After transmitting the last byte of the command string, the AC37 will put the response data into the receive FIFO while holding off the Receive Data Available flag until the entire response is received. If a receive error occurs, or two seconds expire with no data having been received, the Receive Data Available flag is allowed to operate in it's normal manner.

Mode 2:

Reserved for future use.

Mode 3:

Reserved for future use.